ECE336 – MICROPROCESSORS I

WEEK 12

PIC16F84 TIMERS & COUNTERS

WATCHDOG TIMER

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The primary function of the Watchdog Timer (WDT) is to reset the microcontroller, in the event of a software malfunction, by resetting the device if it has not been cleared in software. It can also be used to wake the device from Sleep mode.

The WDT is a free-running timer which uses the low-power RC oscillator and requires no external components. Therefore, the WDT will continue to operate even if the system's primary clock source (e.g., the crystal oscillator) is stopped under normal operation (e.g., in Sleep mode)

WDT OPERATION

When enabled, the WDT will increment until it overflows or “times out”.

A WDT time-out will force a device Reset, except during Sleep modes.

To prevent a WDT Time-out Reset, the user must periodically clear the Watchdog Timer using the instructions, CLRWDT.

If the WDT times out during Sleep modes, the device will wake-up and continue code execution from where the CLRWDT instruction was executed.

In either case, the TO_bit (4_bit of STATUS register) will be set to indicate that the device Reset or wake-up event was due to a WDT time-out.

If the WDT wakes the CPU from Sleep mode, the SLEEP status bit (bit_3 of status register) will also be set to indicate that the device was previously in a Power-Saving mode

STATUS REGİSTER

TO:Time out bit

1= When PIC is energized or CLRWDT is executed.

0= When WDT overflow occurs.

PD: Power down bit

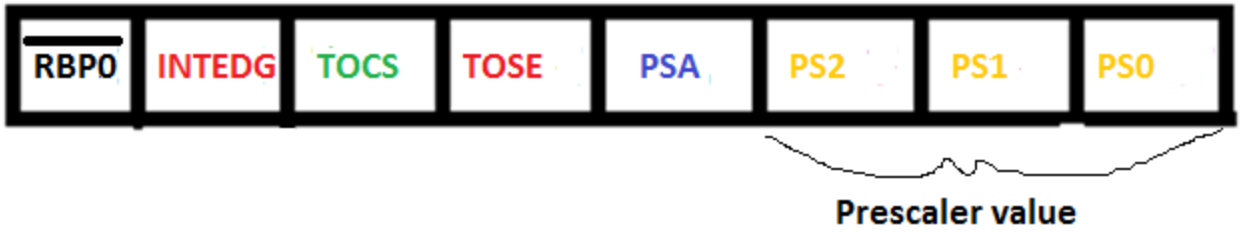
1=When PIC is energized or CLRWDT is executed.

0= When SLEEP command is executed.

OPTION REGISTER

- It is an 8-bit special function register in the RAM. It controls the prescaler value of TMR0 and WDT. The following figure shows the OPTION register with WDT control bits.

OPTION REGISTER



TOCS: TMR0 clock source select bit

1=External clock from RA4/TOCK1

0=Internal clock (Fosc/4 from OSC1)

TOSE: TMR0 source edge select bit

1= Increment on H-to-L transition on RA4/TOCK1

0= Increment on L-to-H transition on RA4/TOCK1

PSA: Prescaler assignment bit,

1=Prescaler is assigned to the WDT

0=Prescaler is assigned to the TMR0

Prescaler value for TMR0 and WDT

Prescaler value	TMR0_rate	WDT_rate
000	1/2	1/1
001	1/4	1/2
010	1/8	1/4
011	1/16	1/8
100	1/32	1/16
101	1/64	1/32
110	1/128	1/64
111	1/256	1/128

- With no prescaler, time-out period of the WDT is 18ms. The table shows the bit assignments with the division rates for the WDT to time out. For exp; 1/128 WDT_rate, time_out period= 128*18ms=2,3 second.

Exp: If presclalar value is b’100’, what is the time out period of WDT.

Sol:

Time out occurs when WDT counts from h’FF’ to h’00’. This takes 18 ms with no prescaler.

If presclalar value is b’100’, WDT_rate= 1/16 (from the table)

Time out period= 16*18ms= 288 ms.

- **Exp:** Write a program to increment the value of PORTB from 00. Every 1152 ms, PORTB get started counting again from 00.